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10/023,117	12/17/2001	Bernardo De Oliveira Kastrup Pereira	NL 000721	2411

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte BERNARDO DE OLIVEIRA KASTRUP PEREIRA and JAN HOOGERBRUGGE

Appeal 2009-002893
Application 10/023,117[1]
Technology Center 2100

Decided: July 13, 2009 [2]

Before HOWARD B. BLANKENSHIP, JOHN A. JEFFERY, and CAROLYN D. THOMAS, *Administrative Patent Judges.*

C. THOMAS, *Administrative Patent Judge.*

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[1] Application filed December 17, 2001. The real party in interest is Koninklijke Philips Electronics N.V.

[2] The two-month time period for filing an appeal or commencing a civil action, as recited in 37 CFR § 1.304, begins to run from the decided date shown on this page of the decision. The time period does not run from the Mail Date (paper delivery) or Notification Date (electronic delivery).

DECISION ON APPEAL

I. STATEMENT OF THE CASE

Appellants appeal under 35 U.S.C. § 134(a) from a final rejection of claims 1-20 mailed on June 7, 2007, which are all the claims remaining in the application. We have jurisdiction under 35 U.S.C. § 6(b).

We affirm.

A. INVENTION

Appellants invented a device and method having a configurable functional unit for executing an instruction according to a configurable function. The configurable functional unit has a plurality of independent configurable logic blocks for performing programmable logic operations to implement the configurable function. Configurable connection circuits are provided between the configurable logic blocks and both the inputs and the outputs of the configurable functional unit. (Spec. 12, Abstract.)

B. ILLUSTRATIVE CLAIM

The appeal contains claims 1-20. Claims 1, 5-7, and 13 are independent claims. Claim 1 is illustrative:

> 1. A data processing device configured according to a device configuration so as to be capable of executing a program comprising an instruction, the device comprising
>
> a configurable functional unit for executing the instruction according to a configurable function that is configured outside the instruction, the configured function including an input ordering instruction, a configured logic function, and an output ordering instruction,

the configurable functional unit including:

a unit input for inputting a plurality of input bits of one or more source registers specified by the instruction,

a unit output for outputting a plurality of output bits to a destination register specified by the instruction,

a first programmable connection circuit that is configured to receive the plurality of input bits and selectively route the input bits to provide a set of logic input bits, based on the input ordering instruction,

a plurality of independent configurable logic blocks for performing programmable logic operations to produce a set of logic output bits corresponding to the configured logic function being applied to the set of logic input bits,

a second programmable connection circuit that is configured to receive the set of logic output bits and selectively route the logic output bits to provide the plurality of output bits, based on the output ordering instruction.

C. REFERENCES

The references relied upon by the Examiner as evidence in rejecting the claims on appeal are as follows:

Abbott US 6,006,321 Dec. 21, 1999
V. Carl Hamacher et al., Computer Organization 19-22 (2d ed. 1984) (hereinafter "Computer Organization")

D. REJECTION

The Examiner entered the following rejection which is before us for review:

Claims 1-20 are rejected under 35 U.S.C. § 102(b) as being anticipated by Abbott.

II. FINDINGS OF FACT

The following findings of fact (FF) are supported by a preponderance of the evidence.

Abbott

1. Abbott discloses that "the transposition circuit 410 includes a set of multiplexers configured to accept input . . . . The set of multiplexers provide optional transposition (i.e., positional interchange) of rotate bit groups between the set of reduction networks in the reduction network bank 212." (Col. 12, ll. 5-14.)

III. PRINCIPLES OF LAW

In rejecting claims under 35 U.S.C. § 102, "[a] single prior art reference that discloses, either expressly or inherently, each limitation of a claim invalidates that claim by anticipation." *Perricone v. Medicis Pharm. Corp.*, 432 F.3d 1368, 1375 (Fed. Cir. 2005), citing *Minn. Mining & Mfg. Co. v. Johnson & Johnson Orthopaedics, Inc.*, 976 F.2d 1559, 1565 (Fed. Cir. 1992).

> Anticipation of a patent claim requires a finding that the claim at issue 'reads on' a prior art reference. In other words, if granting patent protection on the disputed claim would allow the patentee to exclude the public from practicing the prior art, then that claim is anticipated, regardless of whether it also covers subject matter not in the prior art.

Atlas Powder Co. v. IRECO, Inc., 190 F.3d 1342, 1346 (Fed Cir. 1999) (internal citations omitted).

IV. ANALYSIS

Grouping of Claims

In the Brief, Appellants argue claims 1-20 as a group (App. Br. 7-12). For claims 2-20, Appellants essentially repeat the same argument made for claim 1. We will, therefore, treat claims 2-20 as standing or falling with claim 1. *See* 37 C.F.R. § 41.37(c)(1)(vii). *See also In re Young,* 927 F.2d 588, 590 (Fed. Cir. 1991).

The Anticipation Rejection

We now consider the Examiner's rejection of the claims under 35 U.S.C. § 102(b) as being anticipated by Abbott.

Appellants contend that Abbott does not teach that the output of the transposition circuit 410 is provided to a destination register that is specified in an instruction, as specifically claimed in claim 1." (App. Br. 8.) Appellants further contend that

> One of skill in the art would not consider an intermediate transposition circuit that outputs bits to subsequent internal logic circuits and further processing units, as taught by Abbott, to be identical or equivalent to a connection circuit that selectively routes logic output bits to a destination register that is specified in an instruction based on an output ordering instruction, as claimed by the applicants.

(App. Br. 9.)

The Examiner found:

> However, when applicant claims "an input ordering instruction", "a configured logic function", and "a output ordering instruction", the functionality and operation of these claim elements are provided by Abbott's "direct control vector" ("DCV"). This is because as claimed, applicant's "input

> ordering", "configured logic", and "output ordering" instructions/function are claimed as controlling/configuring the operation of applicant's device, in the exact same manner that Abbott's DCV is disclosed as controlling/configuring the device of the prior art.

(Ans. 6.)

Issue: Have Appellants shown that the Examiner erred in finding that Abbott discloses selectively routing the logic output bits to provide the plurality of output bits, based on the output ordering instruction?

The determinative issue in this case turns on whether Abbott discloses selectively routing output bits based on an output ordering instruction.

In essence, Appellants contend that Abbott shows intermediate steps in Figure 4 between the transposition circuit 410 and the destination registers 104/106 of Figure 2, and that such a configuration is distinguishable from the claimed "a second programmable connection circuit that is configured to receive the set of logic output bits and selectively route the logic output bits to provide the plurality of output bits, based on the output ordering instruction." We disagree.

Initially, we note that although Appellants argue that Abbott does not teach that the output of the transposition circuit 410 is provided to a destination register that is specified in an instruction, as specifically claimed in claim 1 (App. Br. 8), the Appellants have chosen to draft the claims, claim 1 in particular, far more broadly. During patent prosecution, claims are construed as broadly as is reasonable. Hence, the claimed "selectively route the logic output bits to provide the plurality of output bits, based on the output ordering instruction" reads on any selective output configuration based on an ordering instruction, not merely a "direct" output from the

connection circuit itself, as seemingly contended by Appellants. In other words, as suggested by the Examiner and endorsed by us, given the open-ended nature of the claim, other elements may be added intermediately to the data flow configuration and still form a construct within the scope of the claim. (*see* Ans. 10.)

For example, the Examiner found that Abbott's Figure 4 discloses that unit 410 provides output bits that flow through unit 412, 414, optional functional unit 214 of Figure 2, to the OUTPUT shown on the right side of Figure 2, which connects to register banks 104 and 106. (Ans. 9-10.) We find that there is nothing in the language of claim 1 to contradict the Examiner's conclusion that claim 1 is open-ended and thus reads on Abbott's output bits flow.

As for the claimed "output ordering instruction," Appellants also contend in the Brief that the Office Action fails to identify where Abbott teaches such an output ordering instruction. (App. Br. 8.) In the Answer, the Examiner found that Abbott provides positional interchange of rotate bit groups where "positional interchange" is a change in the ordering of bits and is an ordering operation. (Ans. 6; FF 1.) Appellants fail to provide any reply to the Examiner's specific findings. Thus, we find the aforementioned Examiner's findings undisputed by Appellants.

Although Appellants group claims 5 and 6 separately in the Brief (App. Br. 10), we find that the arguments pertaining thereto in essence rely on the same arguments presented for claim 1, which we have found unpersuasive.

As for claims 7-12 and 13-20, Appellants merely argue that Abbott neither teaches nor suggests the limitations claimed therein without

providing any meaningful analysis that explains why the Examiner erred. (App. Br. 11.) A statement which merely points out what a claim recites will not be considered an argument for separate patentability of the claim. *See* 37 C.F.R. § 41.37(c)(1)(vii). We note that arguments which Appellants could have made but chose not to make in the Brief have not been considered and are deemed to be waived.

Thus, Appellants have *not* persuaded us of error in the Examiner's conclusion of anticipation for representative claim 1. Therefore, we affirm the Examiner's § 102 rejection of independent claim 1 and of claims 2-20, which fall therewith.

V. CONCLUSIONS

We conclude that Appellants have not shown that the Examiner erred in rejecting claims 1-20.

Thus, claims 1-20 are not patentable.

VI. DECISION

In view of the foregoing discussion, we affirm the Examiner's rejection of claims 1-20.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a). *See* 37 C.F.R. § 1.136(a)(1)(iv) (2009).

AFFIRMED

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